SEARCH REQUEST FORM **Scientific and Technical Information Center - EIC2800**

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Date 5/2/03 Serial # 09/602,395 Priority Application Date 6/22/00

Your Name Thanhha Pham Examiner # 77623

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Where have you searched so far on this case?

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

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What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. 6,436,771

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What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Nitridation ; then oxidation surface with oxide layer & silicon surface to form different thickness gate oxides

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Searcher: _____	Structure (#)_____	STN_____
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US006436771B1

(12) **United States Patent**
Jang et al.

(10) **Patent No.: US 6,436,771 B1**
(45) **Date of Patent: Aug. 20, 2002**

(54) METHOD OF FORMING A SEMICONDUCTOR DEVICE WITH MULTIPLE THICKNESS GATE DIELECTRIC LAYERS

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(22) Filed: Jul. 12, 2001

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(52) U.S. Cl. 438/275; 438/216; 438/279; 438/286; 438/287; 438/528; 438/591; 438/981

(58) Field of Search 438/197, 216, 438/230, 275, 279, 286, 287, 529, 528, 585, 591, 981

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(57) ABSTRACT

Process sequences used to simultaneously form a first dielectric gate layer for a first group of MOSFET elements, and a second dielectric gate layer for a second group of MOSFET elements, with the thickness of the first dielectric gate layer different than the thickness of the second gate dielectric layer, has been developed. A first iteration of this invention entails a remote plasma nitridization procedure used to form a thin silicon nitride layer on a bare, first portion of a semiconductor substrate, while simultaneously forming a thin silicon oxynitride layer on the surface of a first silicon dioxide layer, located on second portion of the semiconductor substrate. A thermal oxidation procedure than results in the formation of a thin second silicon dioxide layer, on the first portion of the semiconductor substrate, underlying the thin silicon nitride layer, while the first silicon dioxide layer, underlying the silicon oxynitride component of the composite dielectric layer, only increases slightly in thickness. A second iteration of this invention features the formation of a silicon nitride—first silicon dioxide, composite gate layer, on a first portion of a semiconductor substrate, with the composite gate layer used to retard oxidation during a thermal oxidation procedure used growth to form a second silicon dioxide layer, on a second portion of the semiconductor substrate

6 Claims, 4 Drawing Sheets